

67,200-409; TSMC 00-661
Serial Number 09/978,420

REMARKS

Favorable reconsideration of this application in light of the following remarks is respectfully requested.

Claims 1-3 and 5-6 are pending within this application. Claim 4 and 13 are canceled herein. Claim 1 is amended herein. No claims have been allowed.

Claim Objections

The Examiner has objected to claim 13 incident to an informality therein.

The Examiner has objected to claim 5 under 37 C.F.R. 1.75(c) as being of improper dependent form for failing to further limit the subject matter of independent claim 1.

In response, applicant has canceled claim 13 and amended claim 1 to delete therefrom the subject matter within claim 1 which corresponds with claim 5.

In light of the foregoing responses, applicant respectfully requests that the Examiner's objection to applicant's claim 5 and claim 13 be withdrawn.

Claim Rejections – 35 U.S.C. § 102

The Examiner has rejected claims 1-6 and 13 under 35 U.S.C. § 102(e) as being anticipated by Wang et al. (U.S. Pub. No. 20020155672 A1; hereinafter "Wang").

In response, and in accord with the above, applicant has canceled claim 13. In further response, applicant has also amended claim 1 to incorporate therein limitations from claim 4, while canceling claim 4. The limitations newly incorporated into claim 1 provide that

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applicant's at least one fuse layer is formed simultaneously with an alignment mark within applicant's microelectronic fabrication.

Applicant notes that the Examiner at page 3, last paragraph, of the office action made FINAL asserts that Wang's bond pad 112b is an alignment mark insofar as Wang's passivation layer 118 is etched aligned with Wang's bond pad 112b.

With the foregoing assertion applicant respectfully disagrees since a person skilled in the art would recognize that an alignment mark within a substrate is employed for aligning a mask with respect to the substrate incident to use of an alignment light beam. Such is not disclosed within Wang. In addition, applicant also asserts that a person skilled in the art would also understand that a bond pad in plan view is generally formed in a square or rectangular shape while an alignment mark in plan view is generally formed in alternative shapes such as but not limited to cross shapes or grid shapes and are thus bond pads and alignment marks are neither functionally nor geometrically equivalent.

Thus, since each and every limitation within applicant's invention as disclosed and claimed within amended claim 1 is not disclosed within Wang, in particular with respect to a fuse formed simultaneously with an alignment mark pad within a microelectronic fabrication, applicant asserts that amended claim 1 may not properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Wang. Since all remaining claims within the foregoing rejection are dependent upon amended claim 1 and carry all of the limitations of amended claim 1, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Wang.

As an additional basis for patentability of applicant's claim 3, applicant asserts that it is atypical (and presumably unanticipated or unobvious) within microelectronic fabrications to form simultaneously a bond pad with an alignment mark.

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In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of claims 1-6 and 13 under 35 U.S.C. § 102(e) as being unpatentable over Wang be withdrawn.

Other Considerations

Applicant again notes the additional prior art of record cited by the Examiner but not employed in rejecting applicant's claims to applicant's invention, in particular: (1) Barth et al. (U.S. Patent No. 6,559,042); (2) Tottori (U.S. Pub. No. 2002/0014680); (3) Ema (U.S. Patent No. 5,297,541); and (4) Tzeng et al. (U.S. Patent No. 6,180,503) as generally pertinent to applicant's invention.

No fee is due as a result of this amendment and response.

SUMMARY

Applicant's invention as disclosed and claimed within amended claim 1 and claim 14 is directed towards a method for fabricating a microelectronic fabrication having formed therein a series of patterned conductor layers and a fuse layer. Within applicant's invention, the fuse layer is formed at a level no lower than a highest of the series of patterned conductor layers. Within one aspect of the invention, the at least one fuse layer is formed simultaneously with an alignment mark within the microelectronic fabrication. Within an additional aspect of the invention, the fuse layer is formed employing a planarizing of a blanket fuse material layer. Absent from the prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure of each and every limitation within applicant's invention.


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CONCLUSION

On the basis of the above remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,


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